

CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (original) A memory array comprising:
 - a. a bitline; and
 - b. a plurality of memory cells, each memory cell having:
 - i. complementary first and second bit nodes storing complementary first and second voltage levels representative of a logic one or a logic zero; and
 - ii. a read amplifier having an amplifier input terminal connected to at least one of the first and second bit nodes, an amplifier output terminal connected to the bitline, and a read-access control terminal.
2. (original) The memory array of claim 1, each memory cell further including:
 - a. a write-access control terminal; and
 - b. a memory access transistor having a first current-handling terminal connected to one of the first and second bit nodes, a second current-handling terminal connected to the bitline, and a control terminal connected to the write-access control terminal.
3. (original) The memory array of claim 1, wherein the read amplifier provides an amplified version of one of the first and second voltage levels on the bitline in response to a read signal on the read-access control terminal.
4. (original) The memory array of claim 1, wherein the memory cell includes first and second cross-coupled inverters, each extending between the first and second bit nodes.

5. (canceled)
6. (previously presented) A memory circuit having a first state representative of a logic zero and a second state representative of a logic one, the memory circuit comprising:
 - a pair of cross-coupled inverters having first and second memory-bit nodes,
 - each node storing a voltage level representative of one of the logic zero and the logic one;
 - a bitline; and
 - a bit-access circuit connected between the bitline and at least one of the first and second memory-bit nodes, the bit-access circuit connecting the bitline and one of the first and second memory-bit nodes during a write operation and maintaining a high impedance between the bitline and one of the first and second memory-bit nodes during a read operation;

wherein the bit-access circuit includes an amplifier having an amplifier input terminal connected to one of the first and second memory-bit nodes, an amplifier output terminal connected to the bitline, and a read-access control terminal.
7. (original) The memory circuit of claim 6, wherein the amplifier includes:
 - a. a first transistor having:
 - i. a first current-handling terminal connected to the bitline;
 - ii. a control terminal connected to the read-access-control terminal; and
 - iii. a second current-handling terminal; and
 - b. a second transistor having:
 - i. a first current-handling terminal connected to the second current-handling terminal of the first transistor;
 - ii. a control terminal connected to the first memory-bit node; and
 - iii. a second current-handling terminal connected to a supply terminal.

8. (previously presented) The memory circuit of claim 6, the bit-access circuit further comprising a memory-access transistor having a first current-handling terminal connected to one of the first and second memory-bit nodes, a second current-handling terminal connected to the bitline, and a control terminal connected to a write-access control terminal.
9. (currently amended) A memory system comprising:
 - a. a bitline;
 - b. a plurality of memory cells, each memory cell including a complementary first and second memory-bit nodes maintaining a complementary first and second voltage levels representative of a data bit; and
 - c. amplifying means connected between the first memory-bit node and the bitline, the amplifying means selectively conveying the first voltage level to the bitline in response to a read-access command.
10. (currently amended) The memory system of claim 9, further comprising means for writing a bitline voltage on the bitline to the first memory-bit node.
11. (original) The memory system of claim 10, wherein the means for writing the bitline voltage comprises a transistor having a first current-handling terminal connected to the bitline, a second current-handling terminal, and a control terminal connected to a write-access control terminal.
12. (currently amended) The memory system of claim 11, wherein the second current-handling terminal is connected to the first memory-bit node.
- 13-15. (canceled)

16. (original) A programmable logic device comprising:
- a. a plurality of configurable resources;
 - b. a bitline; and
 - c. a configuration memory including an array of memory cells, each memory cell having:
 - i. complementary first and second bit nodes storing complementary first and second voltage levels representative of a logic one or a logic zero;
 - ii. a read amplifier having an amplifier input terminal connected to at least one of the first and second bit nodes, an amplifier output terminal connected to the bitline, and a read-access control terminal; and
 - iii. a configuration bit terminal connected to one of the plurality of configurable resources.
17. (original) The programmable logic device of claim 16, each memory cell further including:
- a. a write-access control terminal; and
 - b. a memory access transistor having a first current-handling terminal connected to one of the first and second bit nodes, a second current-handling terminal connected to the bitline, and a control terminal connected to the write-access control terminal.
18. (original) The programmable logic device of claim 16, wherein the configuration bit terminal connects to one of the first and second bit nodes.
19. (original) The programmable logic device of claim 16, wherein the read amplifier provides an amplified version of one of the first and second voltage levels on the bitline in response to a read signal on the read-access control terminal.

20. (original) The programmable logic device of claim 16, wherein the memory cell includes first and second cross-coupled inverters, each inverter extending between the first and second bit nodes.

21. (original) The programmable logic device of claim 16, wherein the programmable logic device further includes a power-on-reset circuit.

22. (original) The programmable logic device of claim 21, wherein the power-on-reset circuit activates the configuration memory at a trip point voltage less than a supply voltage.

23. (original) A programmable logic device (PLD) comprising:

- a. configurable resources; and
- b. a configuration memory storing configuration data defining a configuration of the configurable resources, the configuration memory including:
 - i. a plurality of bitlines; and
 - ii. a plurality of memory cells associated with each bitline, each memory cell having:
 - 1) complementary first and second bit nodes storing complementary first and second voltage levels representative of a logic one or a logic zero; and
 - 2) a read amplifier having an amplifier input terminal connected to at least one of the first and second bit nodes, an amplifier output terminal connected to a respective one of the plurality of bitlines, and a read-access control terminal.

24. (original) The PLD of claim 23, further comprising a non-volatile memory storing the configuration data.

25. (original) The PLD of claim 24, wherein the non-volatile memory is an EEPROM.
26. (original) The PLD of claim 25, wherein the memory cells are static random-memory (SRAM) cells, the SRAM cells providing a shadow random-access memory (RAM).
27. (original) The PLD of claim 25, wherein the PLD is a complex programmable logic device (CPLD).
28. (original) The PLD of claim 25, further comprising:
- a. a plurality of bit latch circuits each connected to a respective one of the plurality of bitlines; and
 - b. a plurality of sense amplifiers each selectively transmitting input signals to a respective one of the plurality of bit latch circuits.
29. (original) The PLD of claim 28, the input signals including EEPROM signals transmitting the configuration data.
30. (original) The PLD of claim 25, further comprising a configuration control circuit controlling the EEPROM and the configuration memory, the configuration control circuit including:
- a. a power-on-reset circuit monitoring a power supply and transmitting an enable signal when the power supply reaches a trip point;
 - b. an address generator generating addresses in response to the enable signal; and
 - c. an address decoder decoding the addresses to provide memory control signals.
31. (original) The PLD of claim 30, wherein the configuration control circuit controls transfer of configuration data from the EEPROM to the configuration memory.